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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,902	08/11/2000	Kozo Harada	50090-234	8376

7590 04/26/2004

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/635,902	HARADA ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22 - 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22 - 24* is/are rejected.

7)☒ Claim(s) *25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on August 4, 2003 has been received and entered in the case.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

Regarding claim 24, the drawings fail to show a second electrode formed on an insulating layer that is on the same surface of the semiconductor chip; the combination of elements must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Regarding claim 25, the drawings fail to show a combined structure of claims 22 and 25 conductive line patterns formed on the both surfaces of the lower semiconductor chip must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

3. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Specification

4. The specification is objected to as failing to provide written description requirement and/or antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: In claim 24, the specification fails to show a second electrode formed on an insulating layer that is on the same surface of the semiconductor chip; the combination of elements must be described in the specification or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim 23 is rejected under 35 U.S.C. 102(b) as being anticipated by Seidler '098.

Regarding claim 23, Seidler discloses in e.g., FIG. 9 a composite semiconductor device structure, comprising at least two semiconductor devices, wherein

- each of said semiconductor devices include:
    - a semiconductor chip (260 or 260');

- at least a first electrode (262 or 262') formed on a first major surface of said semiconductor chip;
- at least a second electrode (264 or 264') formed on a second major surface of said semiconductor chip opposite to said first major surface;
- at least a conductive member (210 or 210') connecting said first electrode to said second electrode and covering a side surface of said semiconductor chip;

- said at least two semiconductor devices are stacked on each other; and
- a conductive member of a lower one of said semiconductor devices (210') is directly connected to a conductive member of an upper one of the semiconductor devices (210).

7. Claims 23 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Komiyama '708.

Regarding claim 23, Komiyama discloses in e.g., FIG. 6 a composite semiconductor device structure, comprising at least two semiconductor devices, wherein

- each of said semiconductor devices include:
  - a semiconductor chip (501a or 501b);
  - at least a first electrode (504a or 504b) formed on a first major surface of said semiconductor chip;
  - at least a second electrode (an area between the bottom-end of the element 510a or 510b and right before the element 533a or 533b) formed on a second major surface of said semiconductor chip opposite to said first major surface;

- at least a conductive member (510a or 510b) connecting said first electrode to said second electrode and covering a side surface of said semiconductor chip;

- said at least two semiconductor devices are stacked on each other; and

- Since Komiyama discloses in Fig. 6 a direct electrical connection by metal bumps (503) between the conductive members of lower and upper one of the semiconductor devices, Komiyama discloses the following limitation "a conductive member of a lower one of said semiconductor devices (510b) is directly connected to a conductive member of an upper one of the semiconductor devices (510a)."

Regarding claim 24, Komiyama discloses in e.g., FIG. 6 a composite semiconductor device structure, comprising at least two semiconductor devices (500a and 500b), wherein

- each of said semiconductor devices include:
  - a semiconductor chip (501a or 501b);
  - at least a first electrode (504a or 504b) formed on a first major surface of said semiconductor chip;
  - an insulating layer (509a or 509b) formed on a second major surface of said semiconductor chip opposite to said first major surface;
  - at least a second electrode (an area between the bottom-end of the element 510a or 510b and right before the element 533a or 533b) formed on said insulating layer;
  - at least a conductive member (510a or 510b) connecting said first electrode to said second electrode and covering a side surface of said semiconductor chip;
- said at least two semiconductor devices are stacked on each other; and

- Since Komiyama discloses in Fig. 6 a direct electrical connection by metal bumps (503) between the conductive members of lower and upper one of the semiconductor devices, Komiyama discloses the following limitation "a conductive member of a lower one of said semiconductor devices (510b) is directly connected to a conductive member of an upper one of the semiconductor devices (510a)."

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seidler in view of Haba et al. '904.

Regarding claim 22, Seidler discloses the claimed invention except for a conductive line pattern formed on said second major surface and extending from the second electrode. However, Haba et al. teaches in e.g., Fig. 11 a conductive line pattern (1012) extending from a second electrode (1010) to an inner electrode (1008). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Seidler by using the conductive line pattern as taught by Haba et al. The one of ordinary skill in the art would have been motivated to modify Seidler in the manner described above for at least the purpose of electrically connecting the central or inner electrode to the redistributed second electrode (column 14, lines 16 – 18).

Allowable Subject Matter

10. Claim 25 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 25 contains allowable subject matter because none of references of record teach or suggest, either singularly or in combination, at least the limitation of a conductive line pattern extending from a first electrode on a first major surface of a lower one of the semiconductor devices being connected via a bump to a conductive line pattern extending from a second electrode on a second major surface of an upper one of the semiconductor devices.

Response to Arguments

11. Applicant's arguments with respect to claims 22 - 24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
4/13/04 7:34:57 PM

BRADLEY BAUMEISTER
PRIMARY EXAMINER